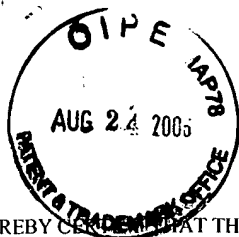


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Cofc



I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED VIA FIRST CLASS MAIL ADDRESSED TO ASSISTANT
COMMISSIONER OF PATENTS ON: August 22, 2006. Depositor: Robert Faber



Signature & Date

| IN THE UNITED STATES PATENT AND TRADEMARK OFFICE | |
|--|---|
| In Re Patent of: Jed H. Rankin, et al. | August 22, 2006 |
| | Examiner: W. David Coleman |
| Patent No. 7,087,499 Issue Date: August 8, 2006 | Group Art Unit: 2823 |
| Title: INTEGRATED ANTIFUSE STRUCTURE FOR FINFET AND CMOS DEVICES | IBM Corporation 2070 Route 52 Dept. 18G, Bldg. 321-482 Hopewell Junction, N.Y. 12533 |

REQUEST TO ISSUE A CERTIFICATE OF CORRECTION OF PATENT
UNDER 37 C.F.R. § 1.322

The Commissioner for Patents
P.O Box 1450
Alexandria, Va 22313-1450

Attn: Certificate of Correction Branch

Certificate
AUG 28 2006
of Correction

Sir:

Patentees respectfully request issuance of the enclosed Certificate of Correction for the above-referenced U.S. Patent.

Upon review of the issued patent, it was noted that the Patent and Trademark Office failed to include three Applicants in the Patent, even though these Applicants were included in the Declaration and Power of Attorney as originally filed

10/539,333

BUR920020082US1

AUG 29 2006

and were not deleted therefrom prior to issue. The Applicants that should be added are Kiran V. Chatty, Robert J. Gauthier Jr., and David M. Fried.

Enclosed, please find a copy of the first page of the US Patent No. 7,087,499.

Since the subject matter of this request for Certificate of Correction was incurred through the fault of the Patent and Trademark Office, Patentees respectfully request issuance of the Certificate of Correction in an expedited manner.

No fee is believed to be due for the submission of this request. However, if any fees are required, please charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "H. Daniel Schnurmann", written over a horizontal line.

H. Daniel Schnurmann
Agent for Applicants
Registration No. 35, 791
Tel. (845) 894-2481



US007087499B2

(12) **United States Patent**
Rankin et al.

(10) Patent No.: **US 7,087,499 B2**
(45) Date of Patent: **Aug. 8, 2006**

(54) **INTEGRATED ANTIFUSE STRUCTURE FOR FINFET AND CMOS DEVICES**

(56) **References Cited**

(75) Inventors: **Jed H. Rankin**, Richmond, VT (US);
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Jeffrey S. Brown, Middlesex, VT (US);
William R. Tonti, Essex Junction, VT (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/539,333**

(22) PCT Filed: **Dec. 20, 2002**

(86) PCT No.: **PCT/US02/41182**

§ 371 (c)(1),
(2), (4) Date: **Jun. 15, 2005**

(87) PCT Pub. No.: **WO2004/059726**

PCT Pub. Date: **Jul. 15, 2004**

(65) **Prior Publication Data**

US 2006/0128071 A1 Jun. 15, 2006

(51) Int. Cl.
H01L 21/76 (2006.01)

(52) U.S. Cl. **438/412; 257/E21.176; 257/E21.205; 257/E21.283**

(58) Field of Classification Search **438/412, 438/431; 257/E21.176, E21.205, E21.283**

See application file for complete search history.

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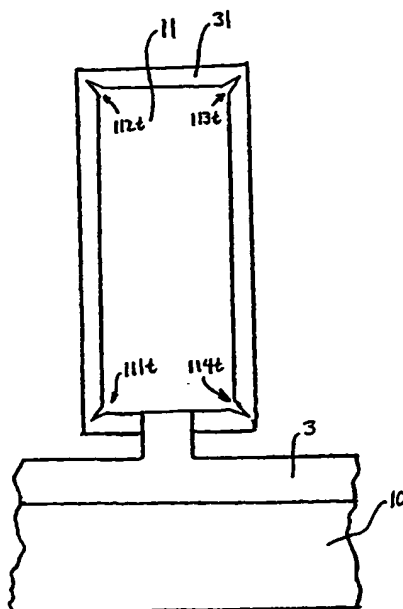
Primary Examiner—W. David Coleman

(74) Attorney, Agent, or Firm—H. Daniel Schnurmann

(57) ABSTRACT

A method is described for fabricating and antifuse structure (100) integrated with a semiconductor device such as a FINFET or planar CMOS device. A region of semiconducting material (11) is provided overlying an insulator (3) disposed on a substrate (10); an etching process exposes a plurality of corners (111–114) in the semiconducting material. The exposed corners are oxidized to form elongated tips (111t–114t) at the corners; the oxide (31) overlying the tips is removed. An oxide layer (51), such as a gate oxide, is then formed on the semiconducting material and overlying the corners; this layer has a reduced thickness at the corners. A layer of conducting material (60) is formed in contact with the oxide layer (51) at the corners, thereby forming a plurality of possible breakdown paths between the semiconducting material and the layer of conducting material through the oxide layer. Applying a voltage, such as a burn-in voltage, to the structure converts at least one of the breakdown paths to a conducting path (103, 280).

17 Claims, 10 Drawing Sheets

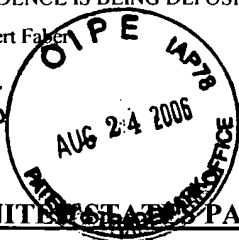


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Robert Faber 8/22/06

Signature & Date



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____ :

August 22, 2006

Jed H. Rankin, et al. _____ :

Examiner: W. David Coleman

Serial No.: 10/539,333 _____ :

Group Art Unit: 2823

Filed: 06/15/2005 _____ :

International Business Machines Corporation
Dept. 18G/Bldg. 321-482
2070 Route 52
Hopewell Junction, NY 12533

Title: INTEGRATED ANTIFUSE
STRUCTURE FOR FINFET
AND CMOS DEVICES

REQUEST FOR CORRECTION OF OFFICIAL FILING RECEIPT

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

Upon receiving the filing receipt (attached) for the above-captioned patent application, it was noted that three of the Applicants were not listed. The Applicants that should be added are Kiran V. Chatty, Robert J. Gauthier Jr., and David M. Fried. Correction is respectfully requested.

Enclosed , please find a copy of the Official Filing Receipt and Delaration and Power of Attorney.

If any fees are required, the Commissioner is hereby authorized to charge such fees to Deposit Account No.

09-0458.

Respectfully submitted,
Jed H. Rankin, et al.

By:

H. Daniel Schnurmann

H. Daniel Schnurmann
Registration No. 35,791
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AUG 29 2006


UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
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| APPL NO. | FILING OR 371 (c) DATE | ART. NO. | FIL FEE REC'D | ATTY. DOCKET NO | DRAWINGS | TOT CLMS | IND CLMS |
|------------|---------------------------|----------|---------------|-----------------|----------|----------|----------|
| 10/539,333 | 06/15/2005 | 2812 | 860 | BUR920020082US1 | 10 | 17 | 2 |

32074
 INTERNATIONAL BUSINESS MACHINES CORPORATION
 DEPT. 18G
 BLDG. 300-482
 2070 ROUTE 52
 HOPEWELL JUNCTION, NY 12533

CONFIRMATION NO. 9276
FILING RECEIPT


OC000000018216047

Date Mailed: 03/10/2006

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Jed H Rankin, Richmond, VT;
 Wagdi W. Abadeer, Jericho, VT;
 Jeffrey S. Brown, Middlesex, VT;
 William R. Tonti, Junction, VT;

Power of Attorney: The patent practitioners associated with Customer Number 45600.

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US02/41182 12/20/2002

Foreign Applications

If Required, Foreign Filing License Granted: 03/06/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US10/539,333**

Projected Publication Date: 06/15/2006

Non-Publication Request: No

Early Publication Request: No

Title

Integrated antifuse structure for finfet and cmos devices

Preliminary Class

438

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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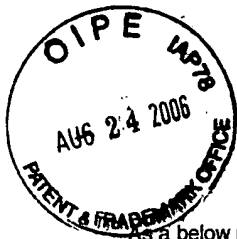
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Declaration and Power of Attorney for Patent Application

As a below named inventor, I hereby declare that::

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
INTEGRATED ANTIFUSE STRUCTURE FOR FINFET AND CMOS DEVICES

the specification of which (check one)

 X is attached hereto.

 was filed on as Application Serial No. and was amended on

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, ' 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, ' 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

| Number | Country | Day/Month/Year | Priority Claimed |
|--------|---------|----------------|------------------|
|--------|---------|----------------|------------------|

I hereby claim the benefit under Title 35, United States Code, ' 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, ' 112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, ' 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

| Serial No.: | Filing Date: | Status: |
|----------------|------------------|-----------|
| PCT/US02/41182 | 20 December 2002 | Completed |

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Customer No. 45600

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 Jay H. Anderson, Intellectual Property Law, IBM Corporation,
 Dept. 18G, Building 321-482, Route 52, Hopewell Junction, New York 12533

Correspondence Address
 Customer No. 32074

Direct Telephone Calls to: Jay H. Anderson - 845-894-3667

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Declaration and Power of Attorney for Patent Application

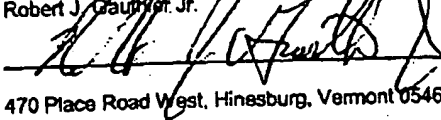
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Citizenship: United States Of America
Post Office Address: Same as residence

AUG 29 2006

Declaration and Power of Attorney for Patent Application

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BUR920020082US1


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Date: _____

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